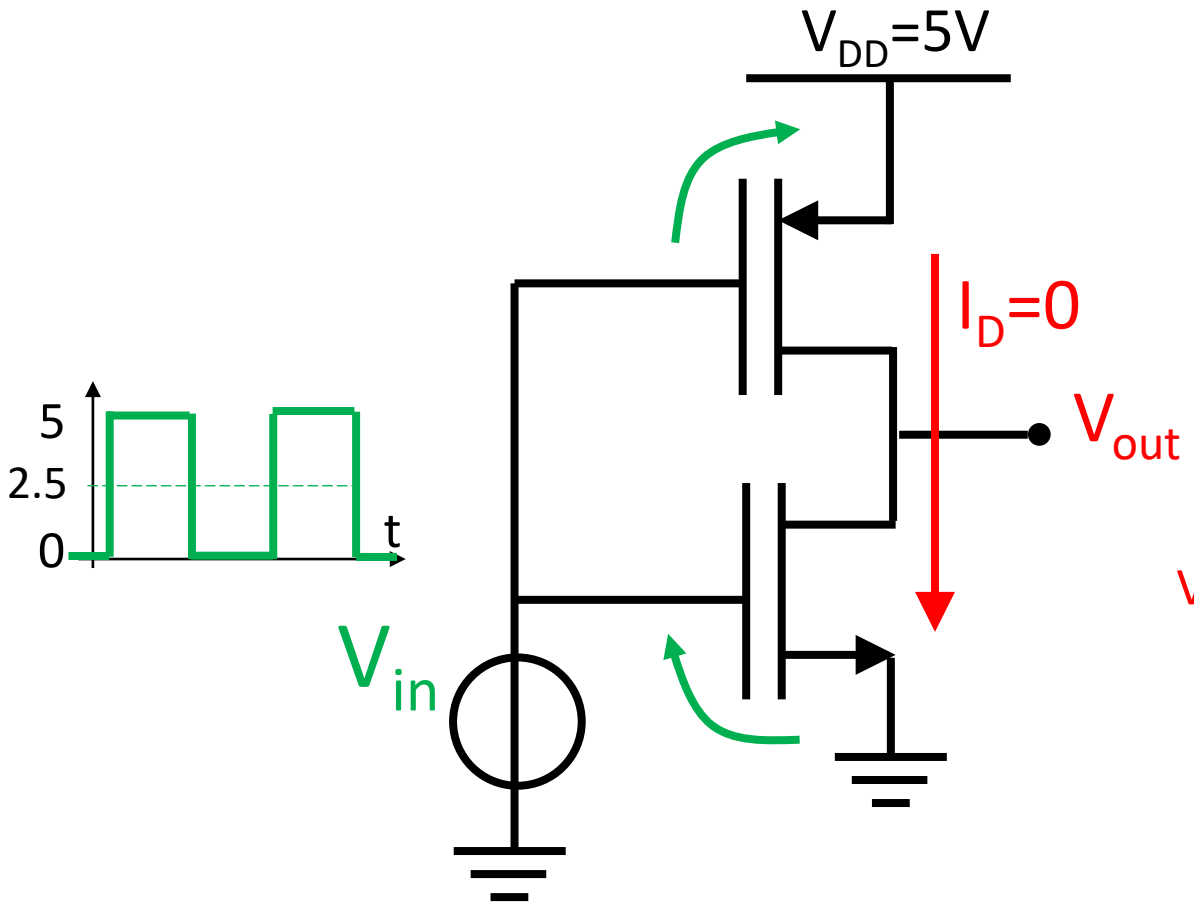
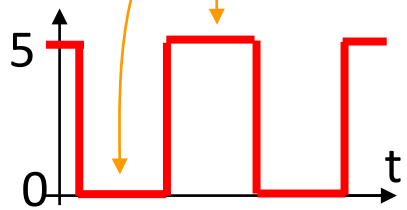
Recap : The CMOS architecture

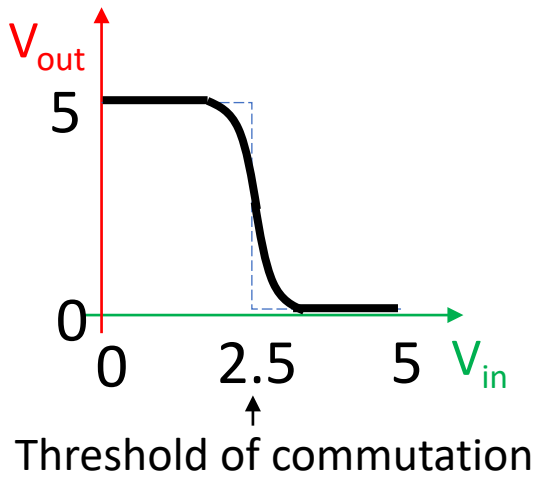




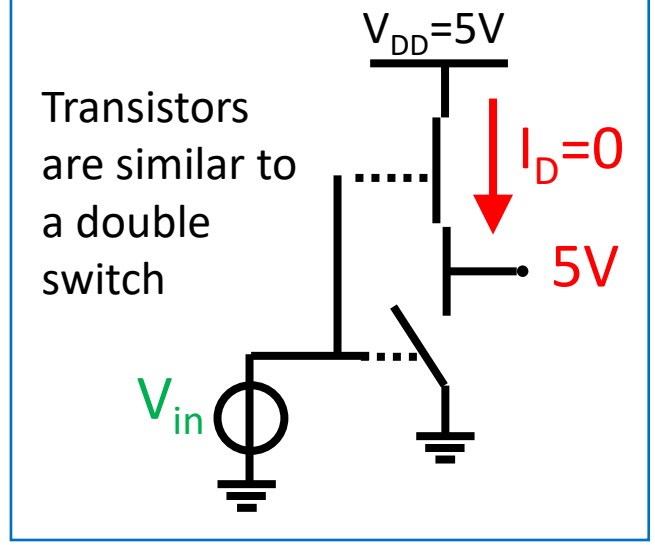
ZERO <u>static</u> power consumption

P $= V_{DD} \cdot I_D =$ **0**

Current always = 0



Transistors are similar to a double switch

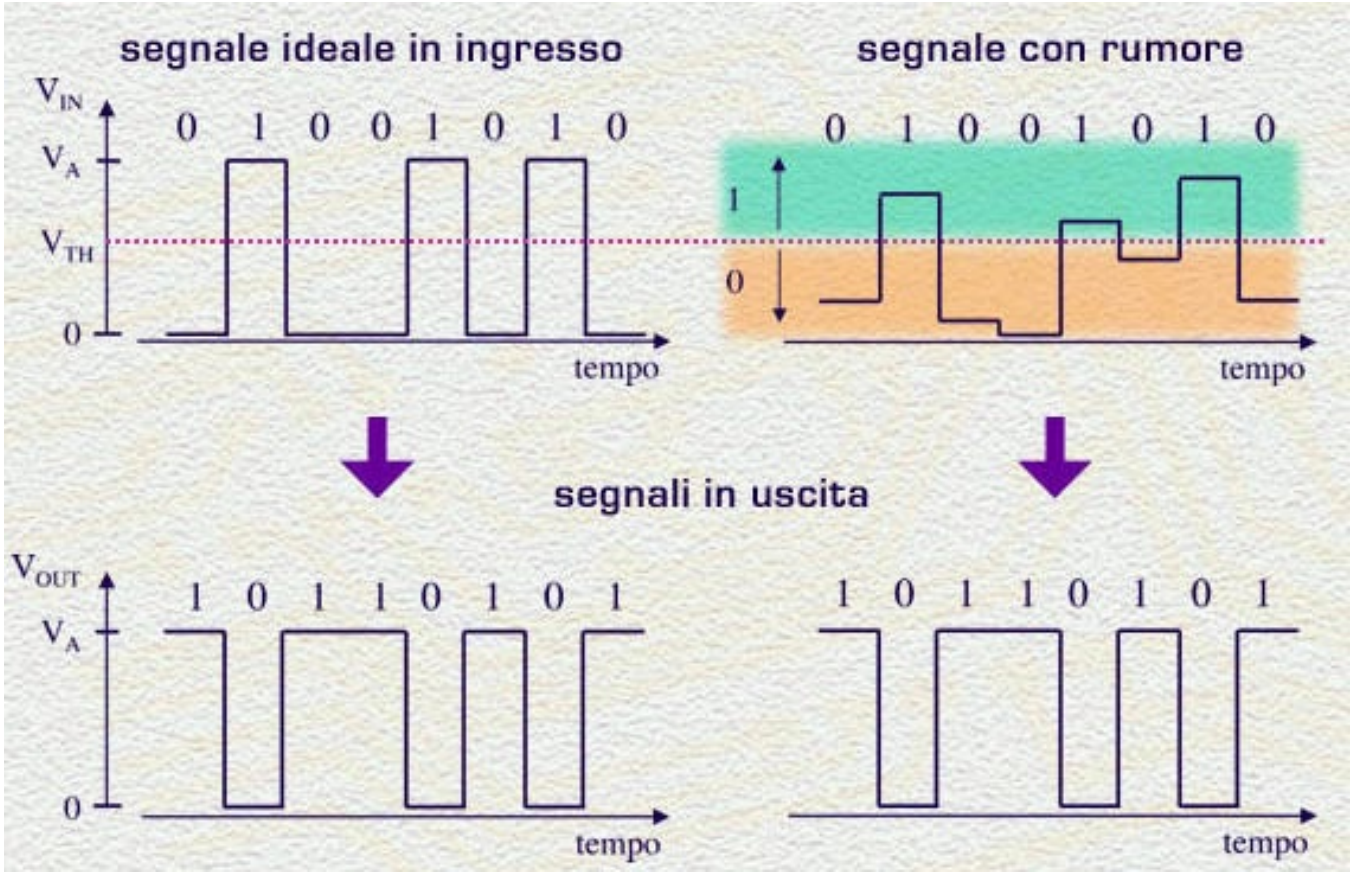


Recap : Immunity to disturbances & reconditioning

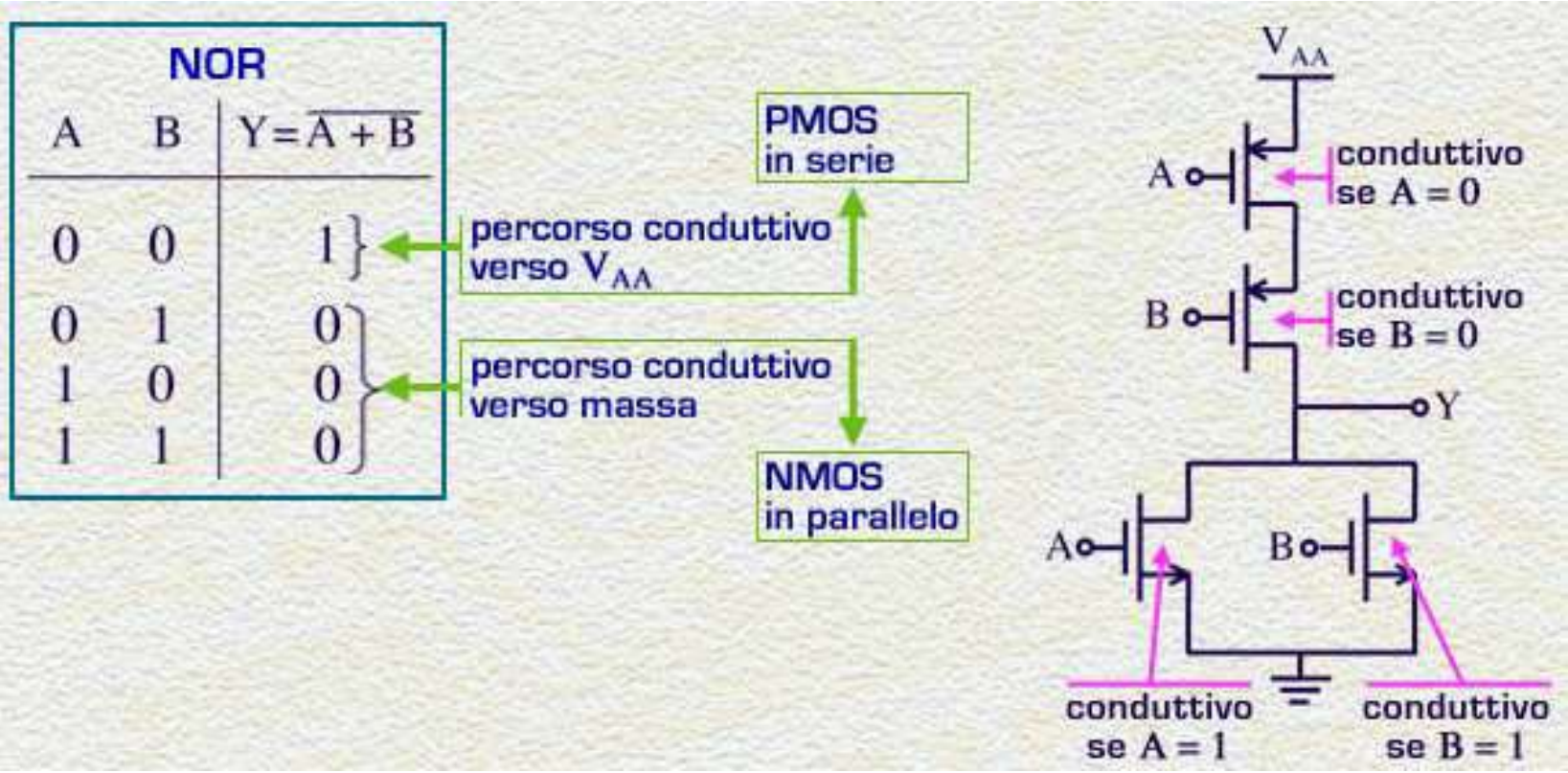
Correct interpretation of the sequence even in the presence of a significant noise level.

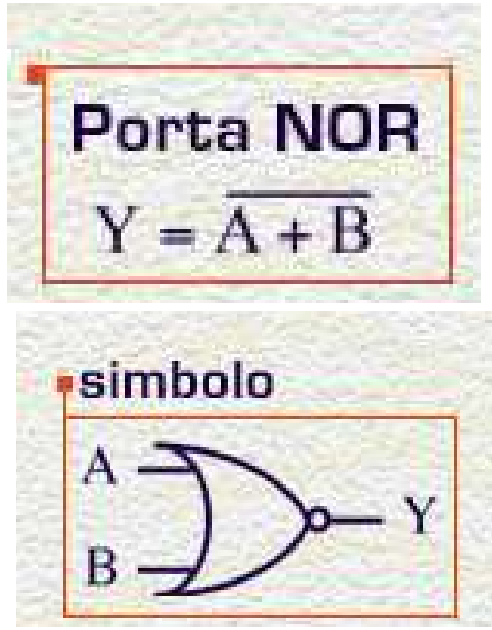
High degree of immunity to disturbances

Reconstruction of the logic levels at output to 0 volts and 5 volts !



CMOS gate as a building block for any Logic Circuit





ELECTRONIC SYSTEMS and TECHNOLOGIES

Master in Management Engineering

Prof. Marco Sampietro

GROUND CONCEPTS ON ELECTRONICS

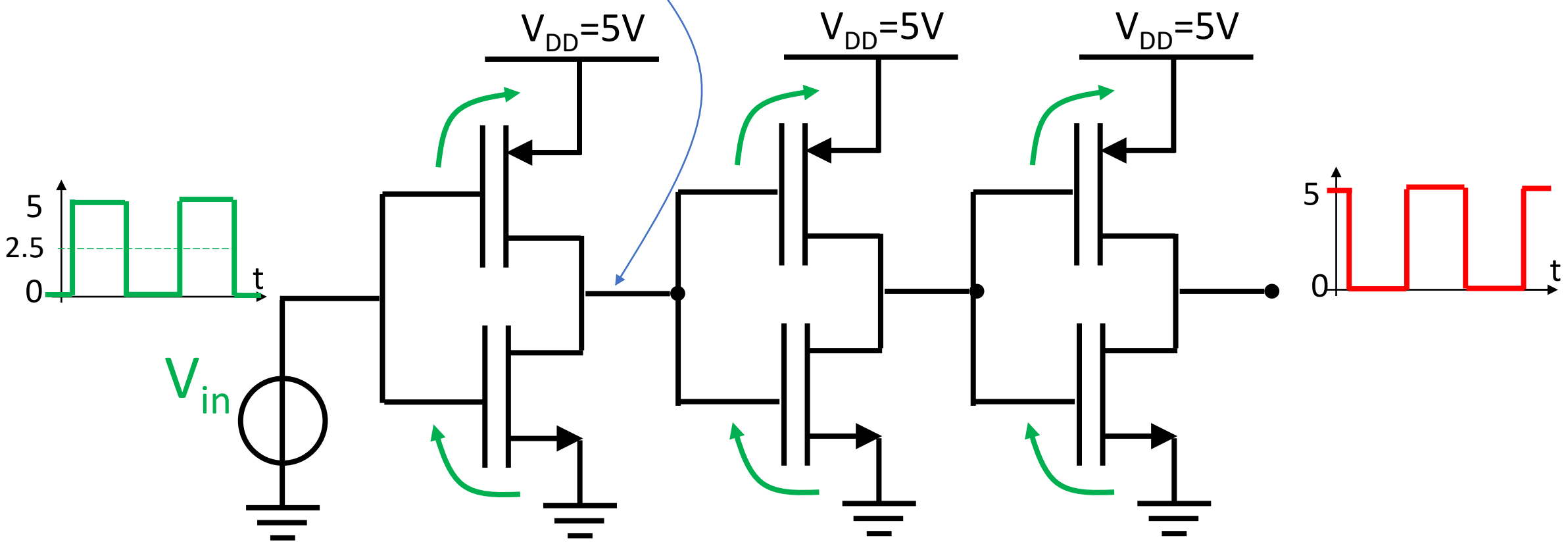
Dynamics of Digital Circuits

Cascading many CMOS inverters

ZERO static power consumption

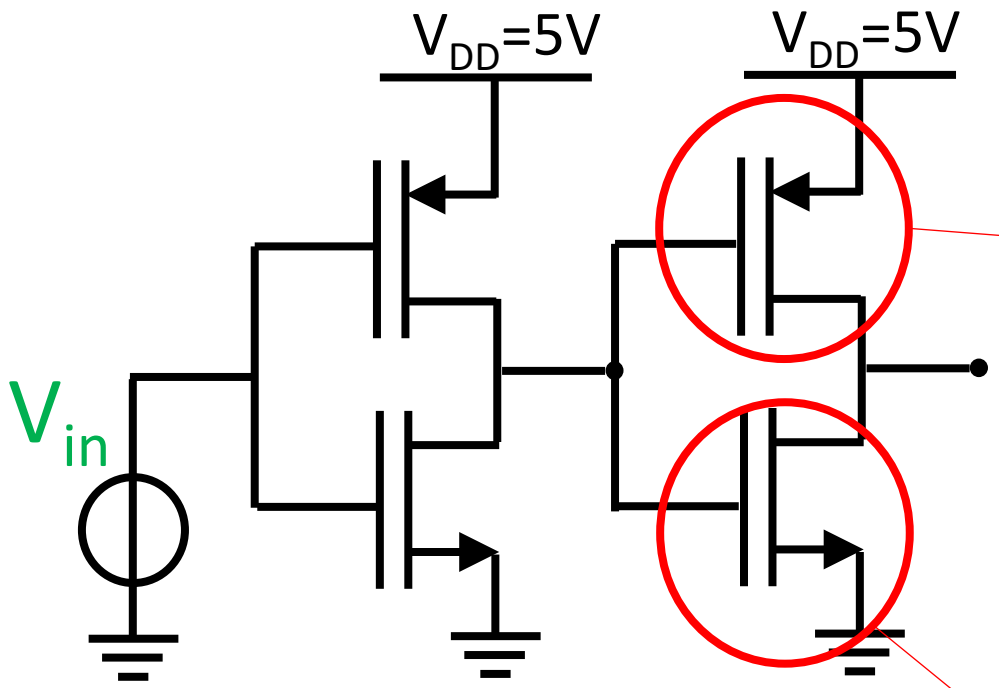
$\mathbf{P} = V_{DD} \cdot I_D = \mathbf{0}$ always

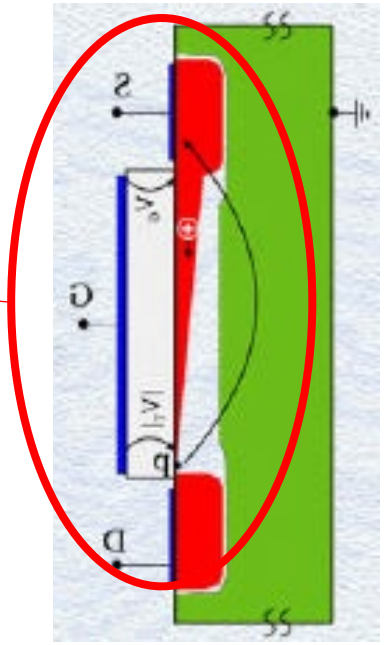
Output of this stage drives the following stage

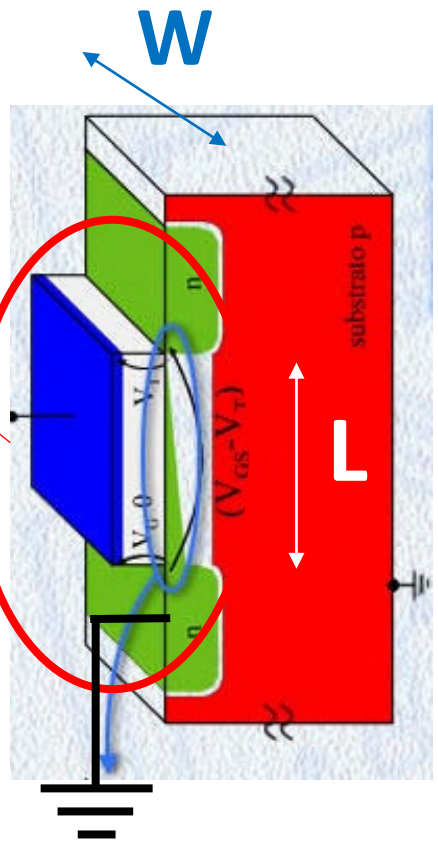


Each CMOS inverter sequentially switch to the new logical state

A closer look to the Gate of a transistor







The Gate of the transistor behaves like a **capacitor**

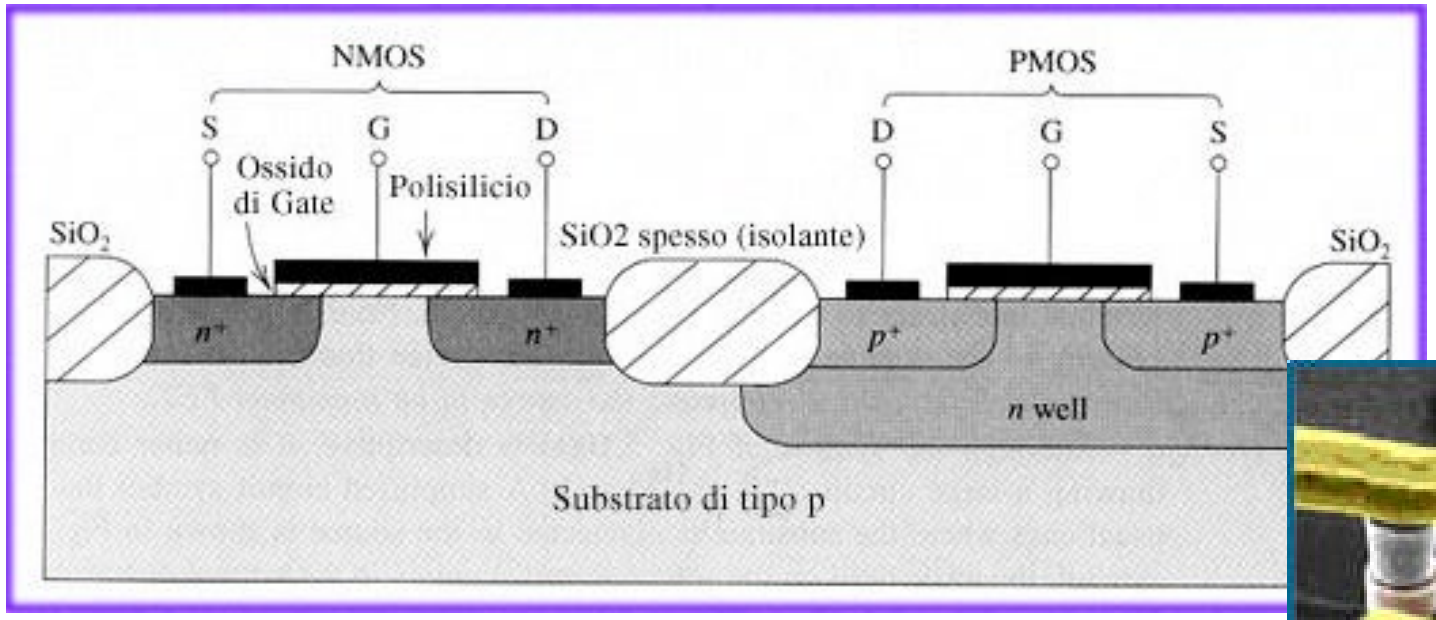
$$C = \frac{\epsilon_0 \cdot \epsilon_r}{X_{ox}} \cdot W \cdot L$$

X_{ox} is the oxide thickness

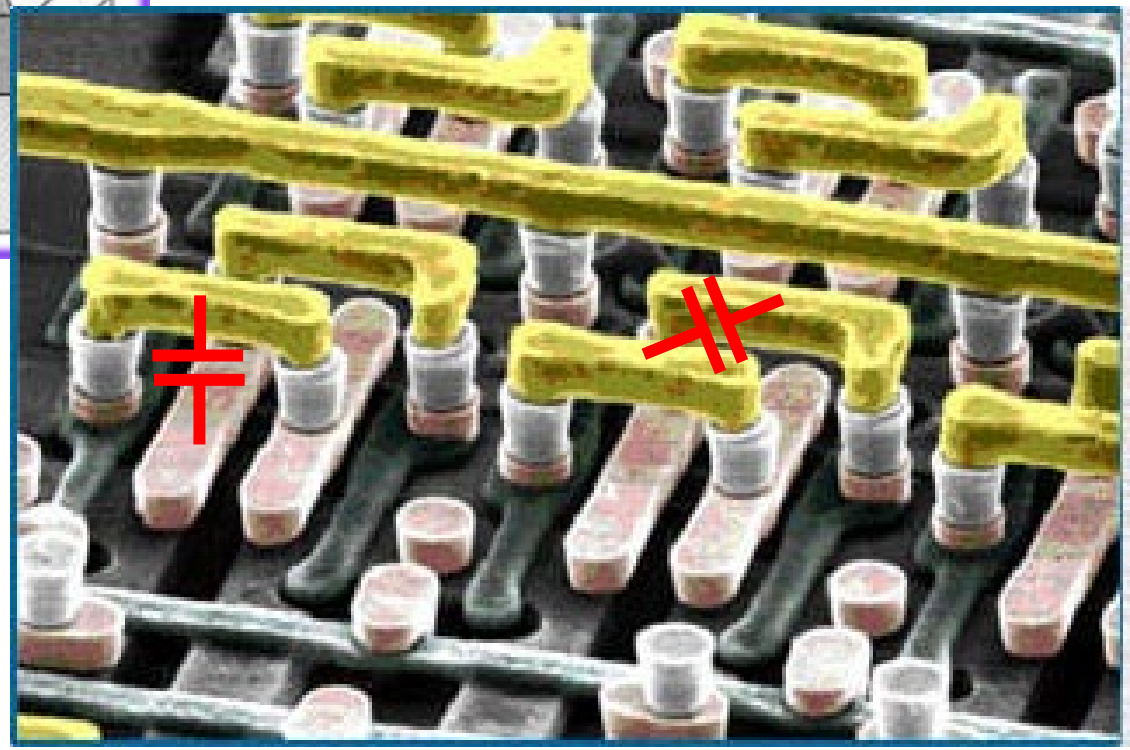
Vacuum permittivity, $\varepsilon_0 = 8.854 \cdot 10^{-12}$ $\left[\frac{Q}{V \cdot m}\right]$

SiO_2 relative permittivity, $\varepsilon_r = 3.9$

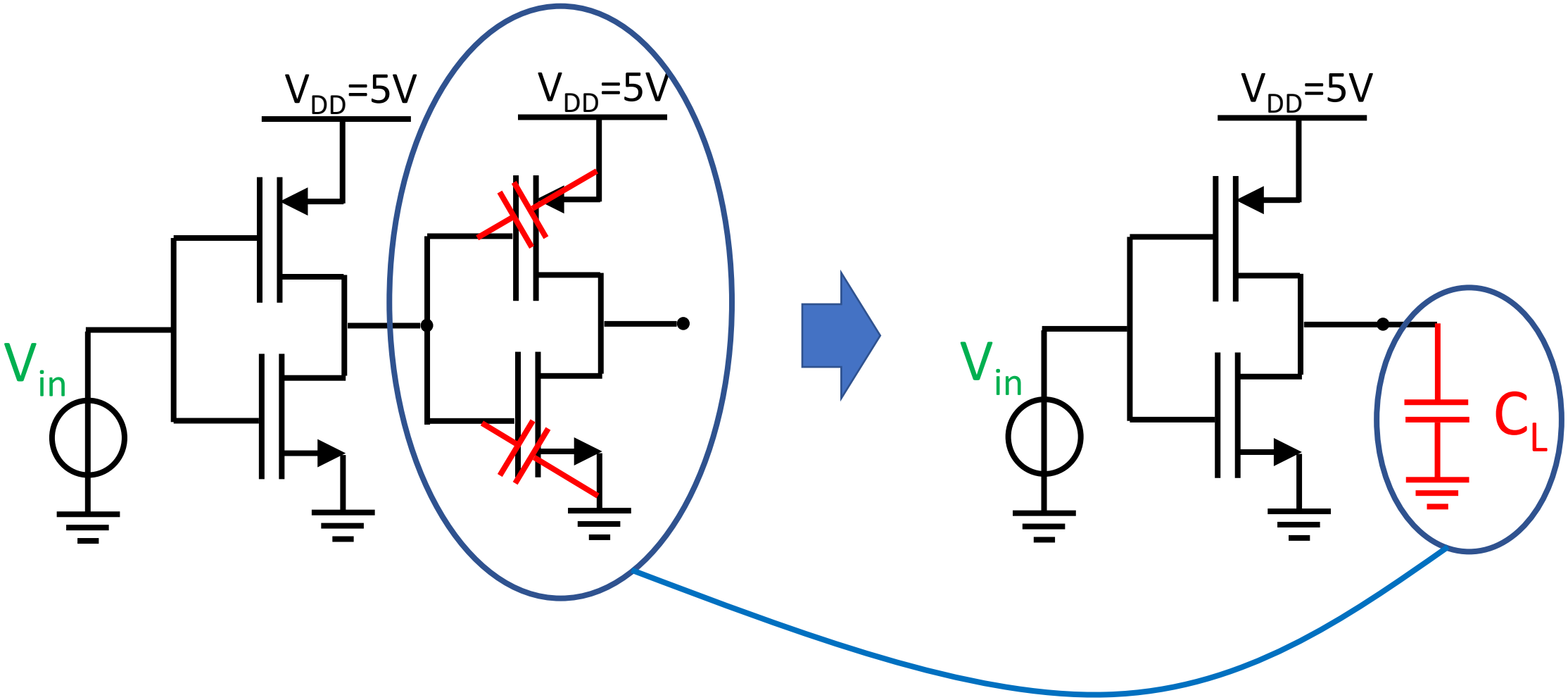
Connections among transistors are also capacitors



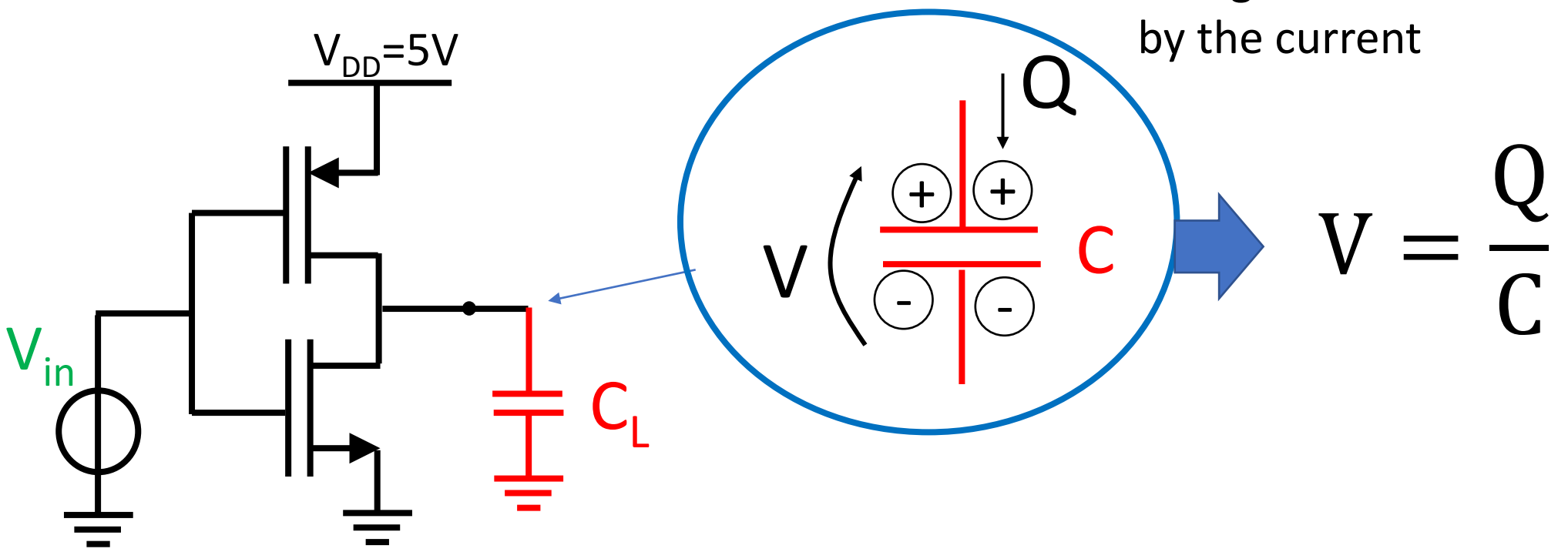
Any metal wire is like a plate of a capacitor, the other plate being another metal around or the ground somewhere



Capacitive load of a CMOS inverter



Charge-Voltage relation on a Capacitor



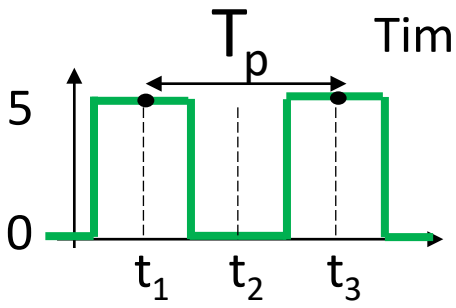
Charge Q is delivered by the current

$$V = \frac{Q}{C}$$

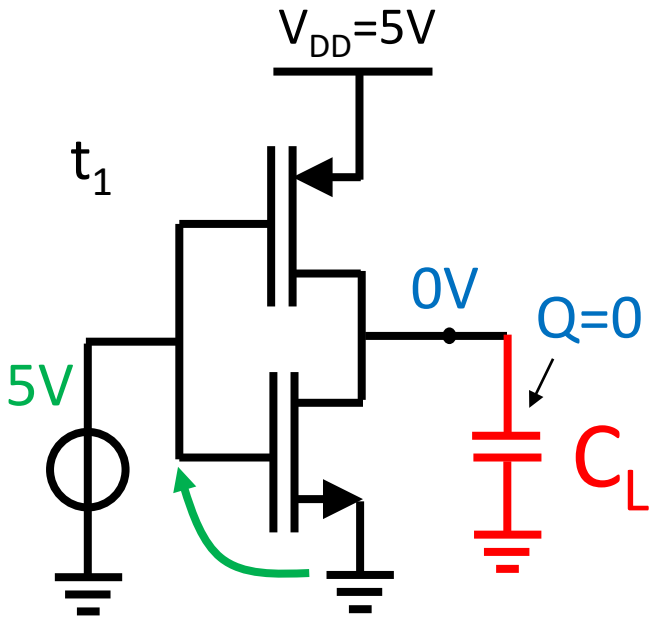
Any node in an electronic circuit can change its voltage only when a charge is provided or removed

Dynamics of the CMOS inverter

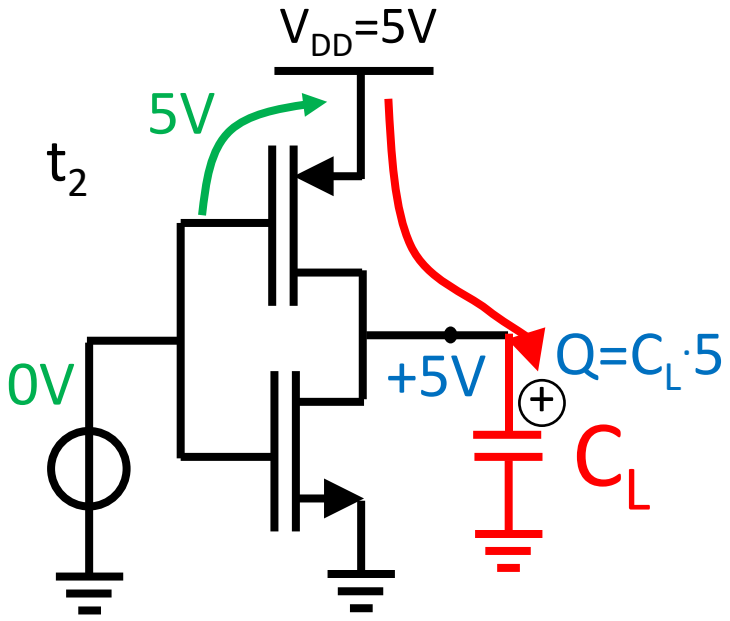
$$V = \frac{Q}{C}$$



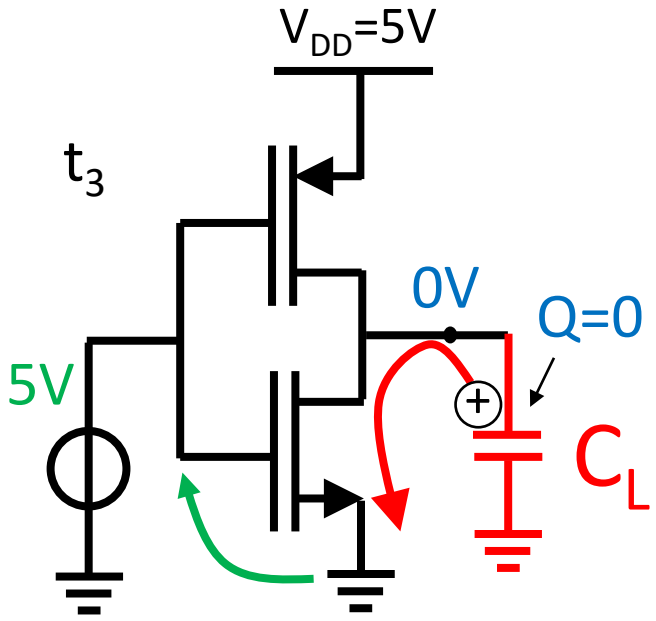
Time period of the digital signal



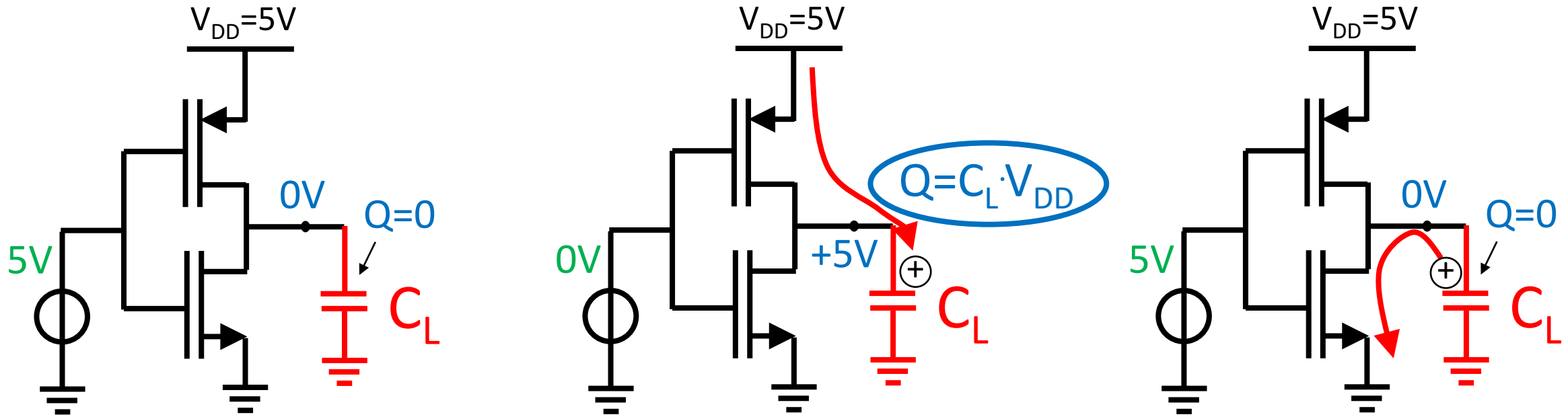
Charge Q is carried by pMOSFET current to C_L



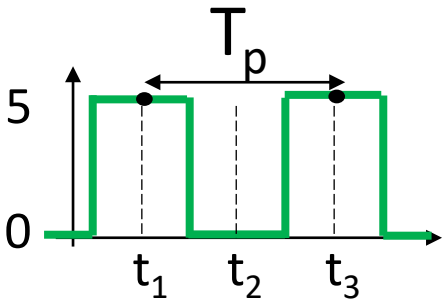
Charge Q is cleared by nMOSFET to ground



Dinamic Power consumption of a CMOS



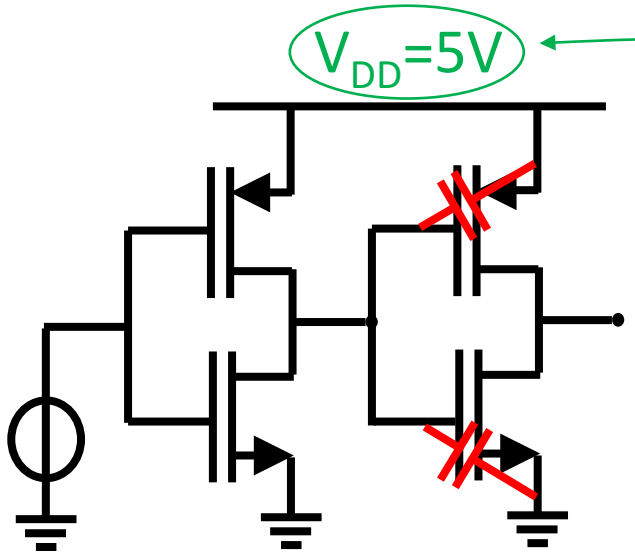
Charge Q started at V_{DD}=+5V and finished to ground in the time of a period T_p



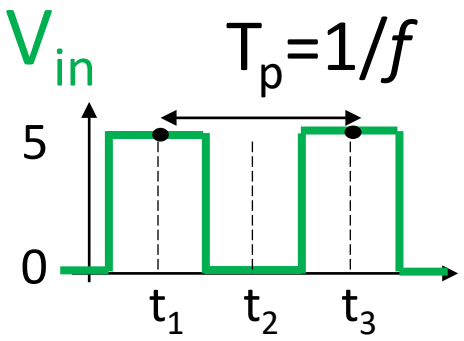
$$P\Big|_{T_p} = V_{DD} \cdot \frac{Q}{T_p} = V_{DD} \cdot C \cdot V_{DD} \cdot \frac{1}{T_p} = V_{DD}^2 \cdot C \cdot f$$

How many times in 1 second ? $f = \frac{1}{T_p}$

Design considerations to manage Power consumption



$$P\big|_{T_p} = V_{DD}^2 \cdot C \cdot f$$



Big advantage in reducing Voltage Supply
5V →3.3V→1.9V→…

BUT :
Reduces Noise margin (see previous lesson)

and …. (see next)

CMOS with minimum dimensions
90nm →26nm→11nm→…

Connections btwn CMOS as short as possible

The total capacitance at the Drain node to ground is important

Linearly increase with frequency of operation (today 3.7GHz).

In portable computer clock frequency can be reduced to save power.

A trade btwn Frequency and Power

Example 1

My desktop computer is more than 10 years old and uses a CPU manufactored with a 32nm technology (minimum feature size) on an oxide thickness x_{ox}=8nm. The CPU is powered at a Voltage Supply V_{DD}=3.3V and operated at a clock frequency of f=2.6GHz. Find the power consumption of one single CMOS inverter.

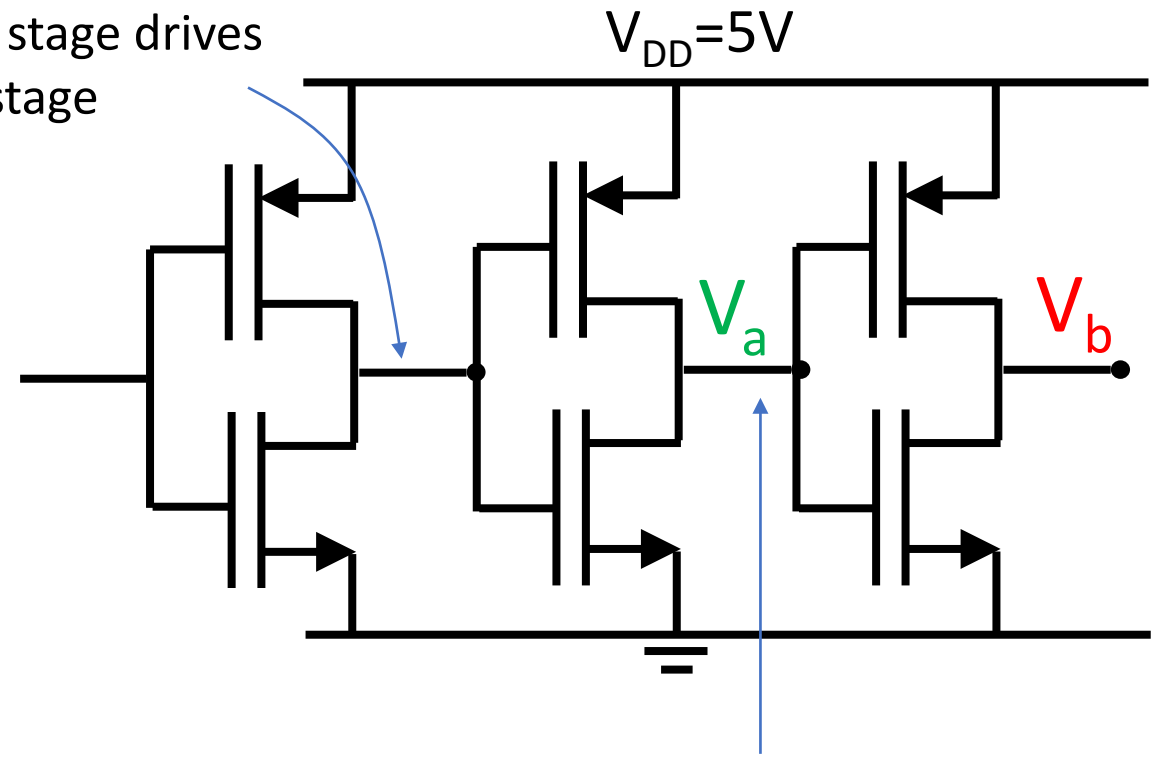
If the CPU dissipates about 100W, how many CMOS inverters are operating at the same time ?

Example 2

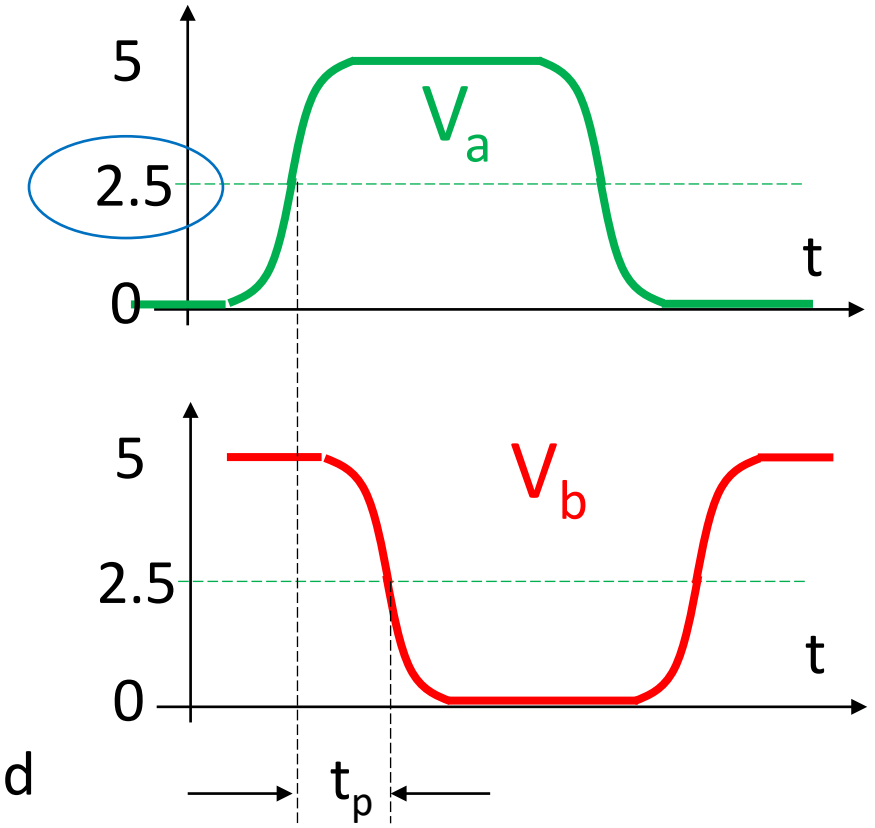
Computers have not increased much the clock frequency through the years, being steady around f_{ck}=3.8GHz. Instead, feature size has diminished a lot, down to 6nm (with x_{ox}=2nm) and voltage supply is 0.9V.
How much power would consume 400 millions of digital inverters ?

Propagation time (Delay) of a logic gate

Output of one stage drives the following stage



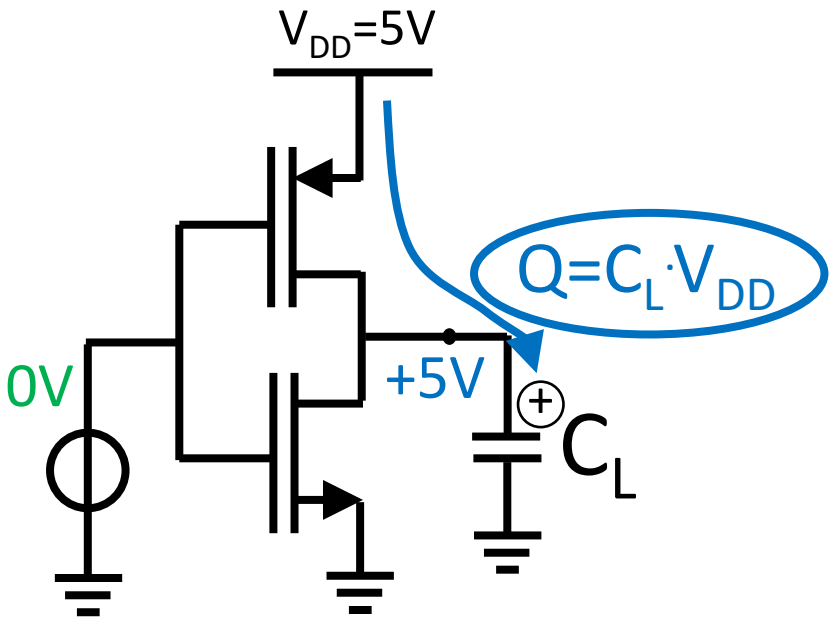
When $V_{DD}/2$ is reached, the next inverter has switched

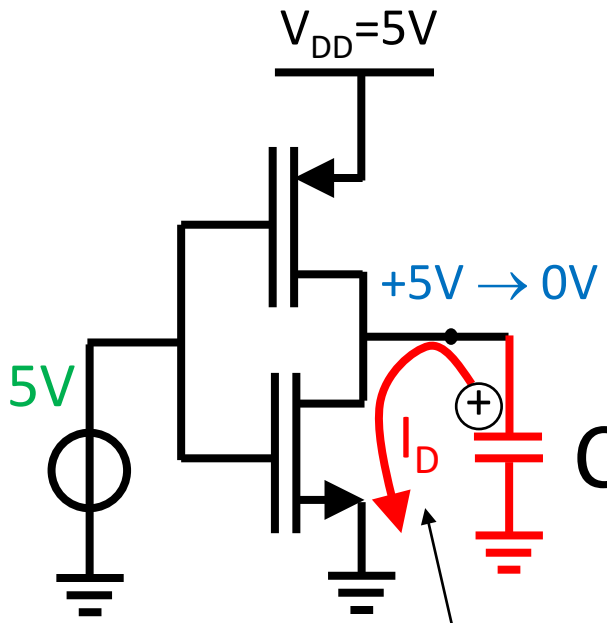


Delay time t_d of the inverter

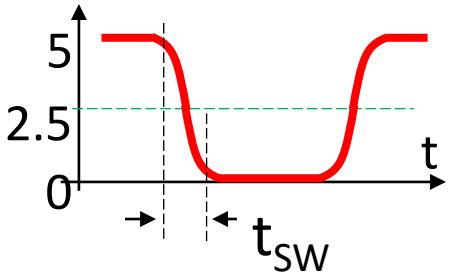
How fast is the switching ?

$$I = \frac{Q}{t}$$





To switch you have to remove the charge on C_L



For simplicity, consider I_D constant all the time at $I_D=k(V_{GS}-V_T)^2$

$$t_{sw} = \frac{Q}{I_D} \cong \frac{C_L \cdot V_{DD}}{k(V_{GS}-V_T)^2} = \frac{\frac{\varepsilon_{ox}}{x_{ox}} W \cdot L \cdot V_{DD}}{\frac{1}{2}\mu \frac{\varepsilon_{ox}}{x_{ox}} \frac{W}{L} (V_{DD}-V_T)^2} = \frac{L^2 \cdot V_{DD}}{\frac{1}{2}\mu (V_{DD}-V_T)^2}$$

Small transistors (again)

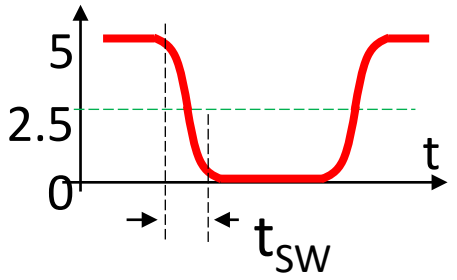
Voltage supply NOT too small

Example 3

Let us consider again a very advanced computer having a CPU with 6nm technology (with x_{ox}=2nm), transistors with a threshold voltage V_T=0.45V and voltage supply of 0.9V.

Estimate the switching time, t_{SW}, of each CMOS gate.

$$t_{sw} = \frac{Q}{I_D} = \frac{L^2 \cdot V_{DD}}{\frac{1}{2}\mu(V_{DD} - V_T)^2}$$



End of the lesson