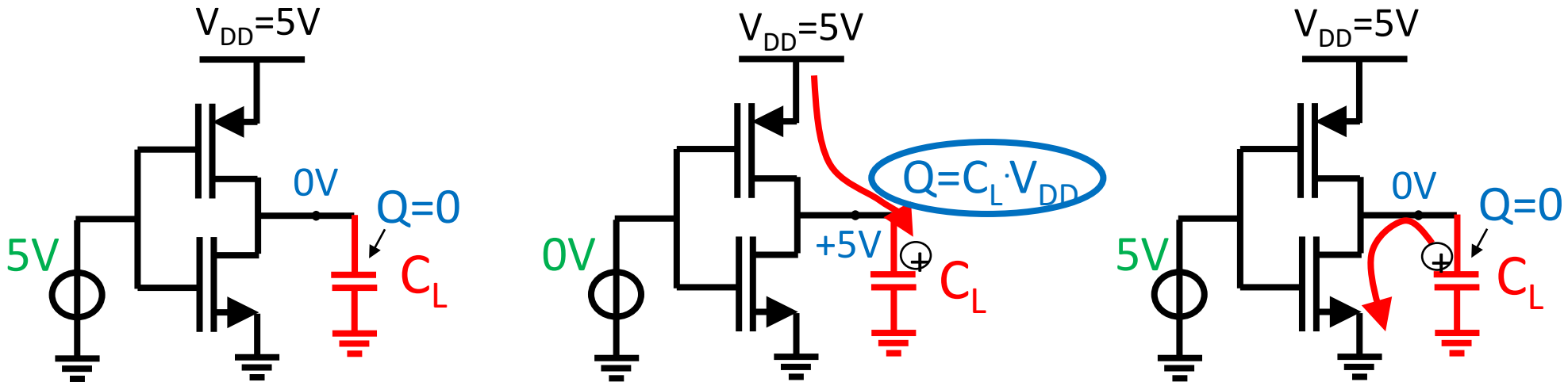
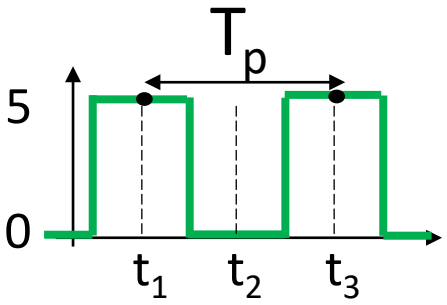
Recap : Dinamic Power consumption of a CMOS



Charge Q started at V_{DD}=+5V and finished to ground in the time of a period T_p



$$P\big|_{T_p} = V_{DD}^2 \cdot C \cdot f$$

Linearly increase with frequency of operation (today 3.7GHz).

90nm → 26nm → 11nm → …

Connections btwn CMOS as short as possible

5V →3.3V→1.9V→…

BUT : Reduces Noise margin

Example 1

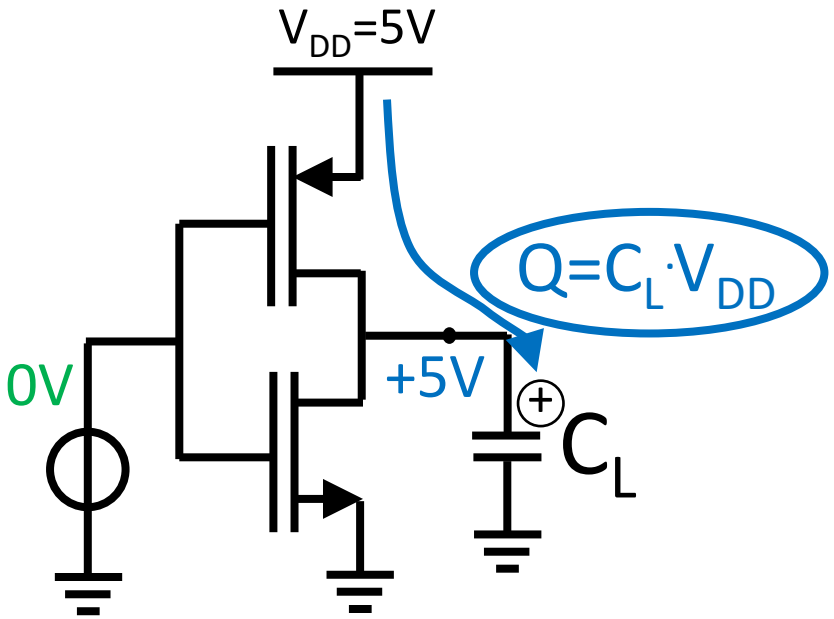
A microprocessor dissipates 25W when it works at a clock frequency f_{ck}=1.2GHz and 18W when working at f_{ck}=600MHz. Calculate the static power dissipated by the processor.

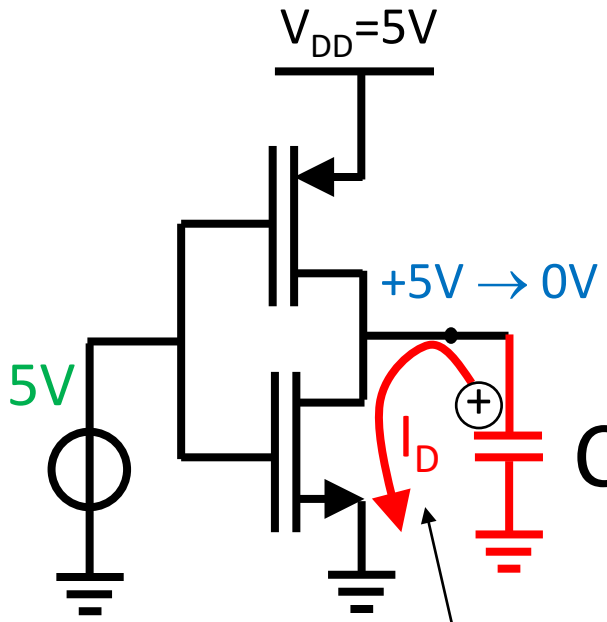
The power dissipated statically by the microprocessor is independent of the frequency of operation.

Instead, the dynamic power has a linear dependence on frequency as $\mathrm{P}\Big|_{\mathrm{T_p}} = V_{DD}^2 \cdot \mathrm{C} \cdot f$

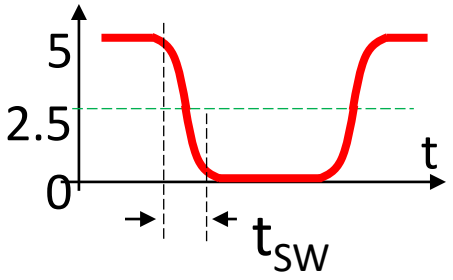
Recap : Switching time of a CMOS inverter

$$I = \frac{Q}{t}$$





To switch you have to remove the charge on C_L



For simplicity, consider I_D constant all the time at $I_D=k(V_{GS}-V_T)^2$

$$t_{sw} = \frac{Q}{I_D} \cong \frac{C_L \cdot V_{DD}}{k(V_{GS}-V_T)^2} = \frac{\frac{\varepsilon_{ox}}{x_{ox}} W \cdot L \cdot V_{DD}}{\frac{1}{2}\mu \frac{\varepsilon_{ox}}{x_{ox}} \frac{W}{L} (V_{DD}-V_T)^2} = \frac{L^2 \cdot V_{DD}}{\frac{1}{2}\mu (V_{DD}-V_T)^2}$$

Small transistors (again)

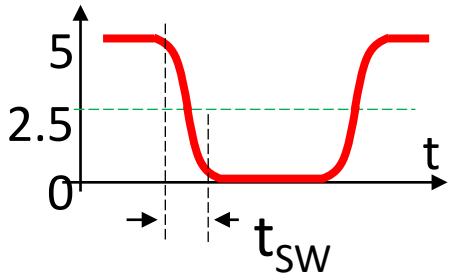
Voltage supply NOT too small

Example 2

Let us consider again a very advanced computer having a CPU with 6nm technology (with x_{ox}=2nm), transistors with a threshold voltage V_T=0.45V and voltage supply of 0.9V.

Estimate the switching time, t_{SW}, of each CMOS gate.

$$t_{sw} = \frac{Q}{I_D} = \frac{L^2 \cdot V_{DD}}{\frac{1}{2}\mu(V_{DD} - V_T)^2}$$



ELECTRONIC SYSTEMS and TECHNOLOGIES

Master in Management Engineering

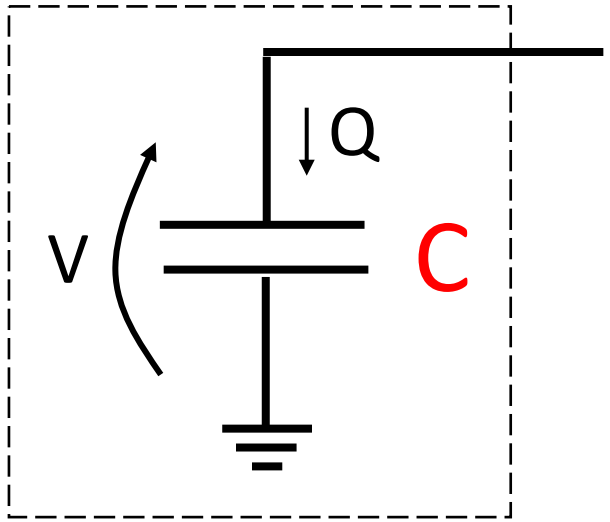
Prof. Marco Sampietro

GROUND CONCEPTS ON ELECTRONICS

Memory devices - DRAM

The capacitor as a memory device

$$V = \frac{Q}{C}$$



Memory cell

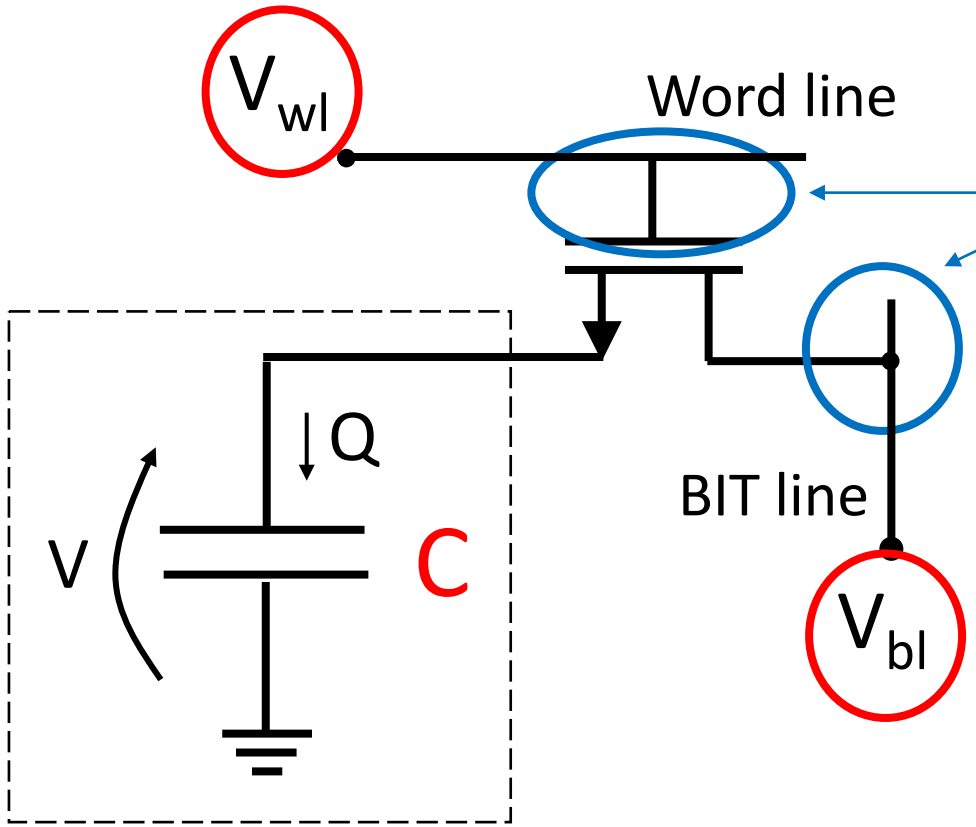
Charge IN → V up → Logic 1

Charge Q=0 → V=0V → Logic 0

How to **write** and/or **read** the capacitance ?

Transistor as a switch to access the Capacitor

$$V = \frac{Q}{C}$$

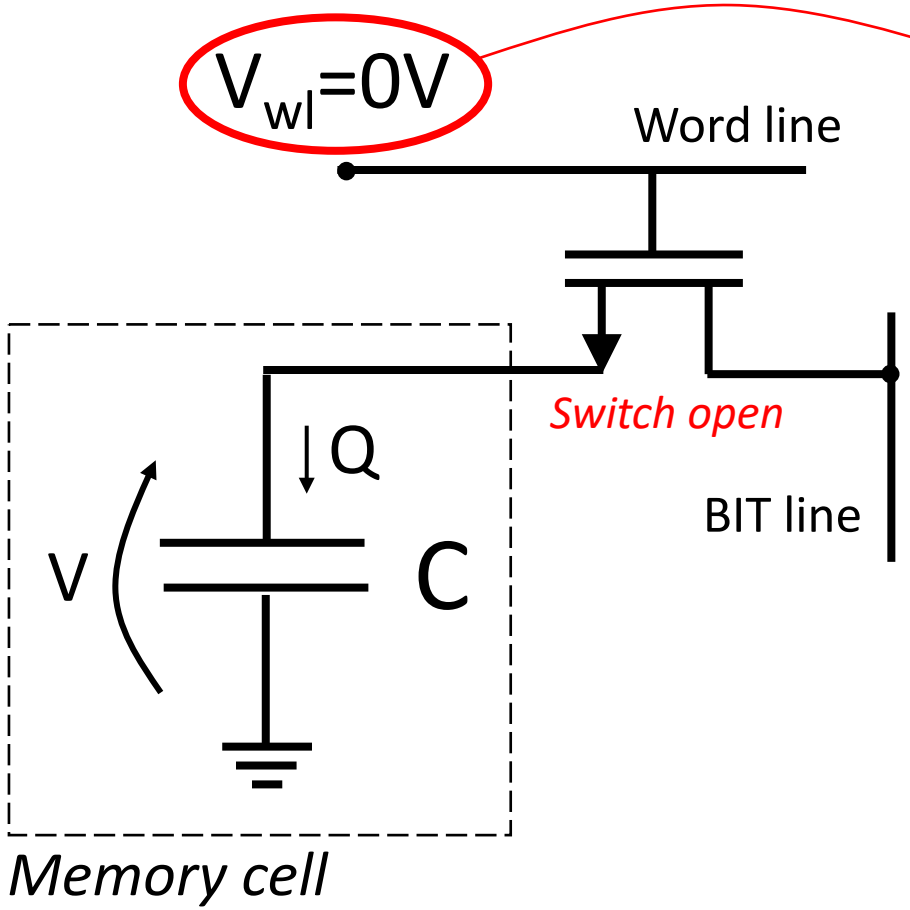


Many memory cells require many switch transistors :

- All Drains in a colum are connected together (BIT LINE)
- All Gates in a row are connected together (WORD LINE)

Voltages V_{wl} and V_{bl} determine the operation of the switch

Memory cell disconnected : storage of information



nMOS is OFF
(independently of C value, 0 or 1 logic)

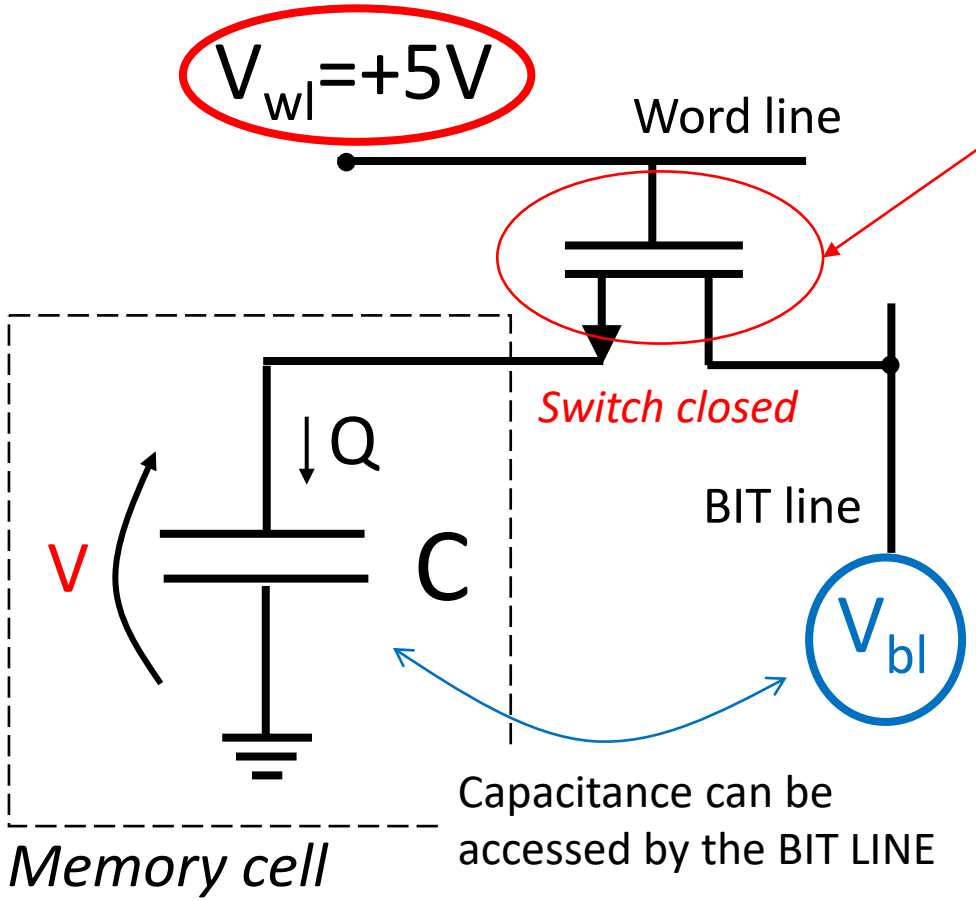
Capacitor is disconnected

Capacitor mantains its value

Charge in C can not be modified by the BIT line

Memory cell connected : switch closed

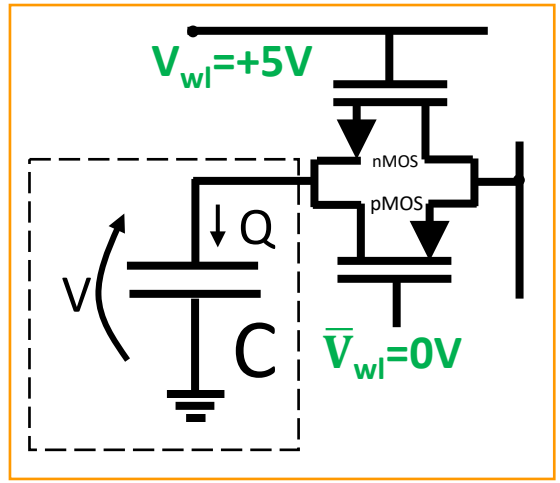
V_T=0.8V and K=7mA/V²



Reading on the BIT LINE :

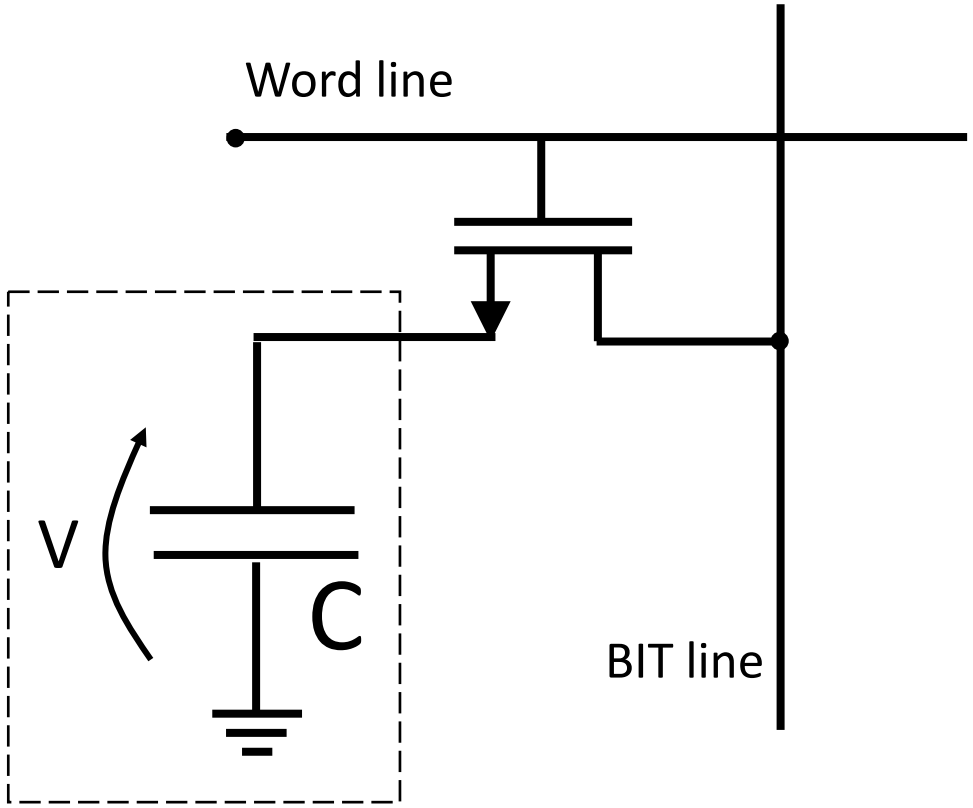
V=0V	V_{bl}=0
V=1V	V_{bl}=1V
V=2V	V_{bl}=2V
V=3V	V_{bl}=3V
V=4.2V	V_{bl}=4.2V
V=5V	~~V_{bl}=4.2V~~ V_{bl}=5V

Solved by :

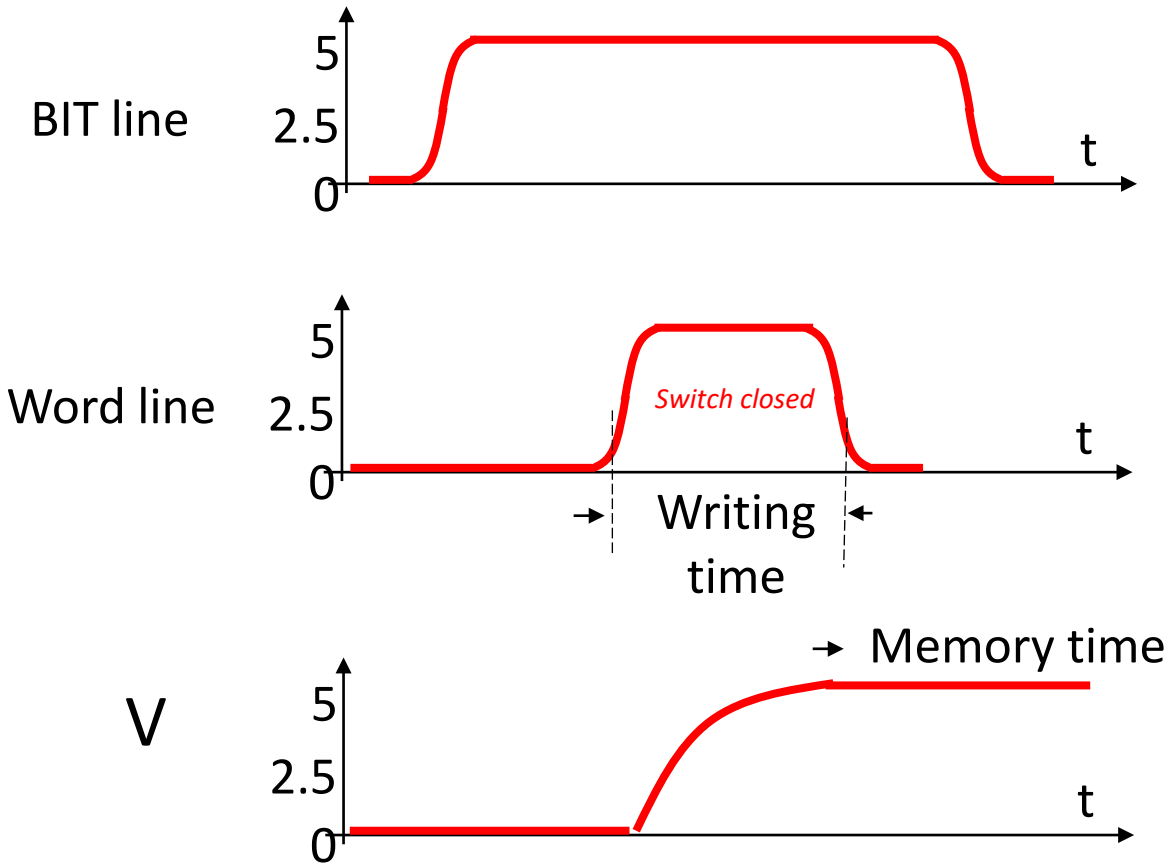


Charge in C can be modified by the BIT line, by a proper voltage V_{bl} (0 or 5V).

Example of writing a «1»

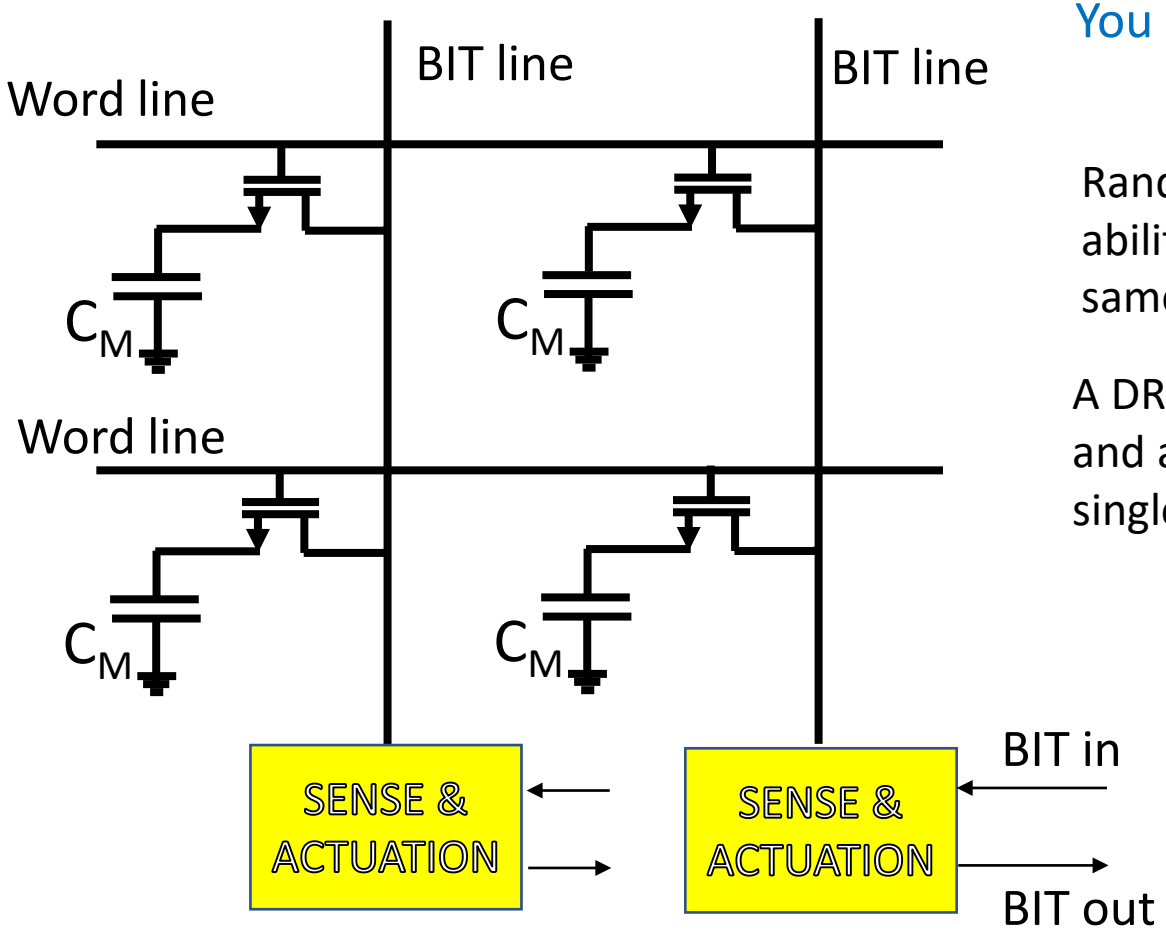


Memory cell



DRAM – Dynamic Random-Access Memory

You can address any cell at your will

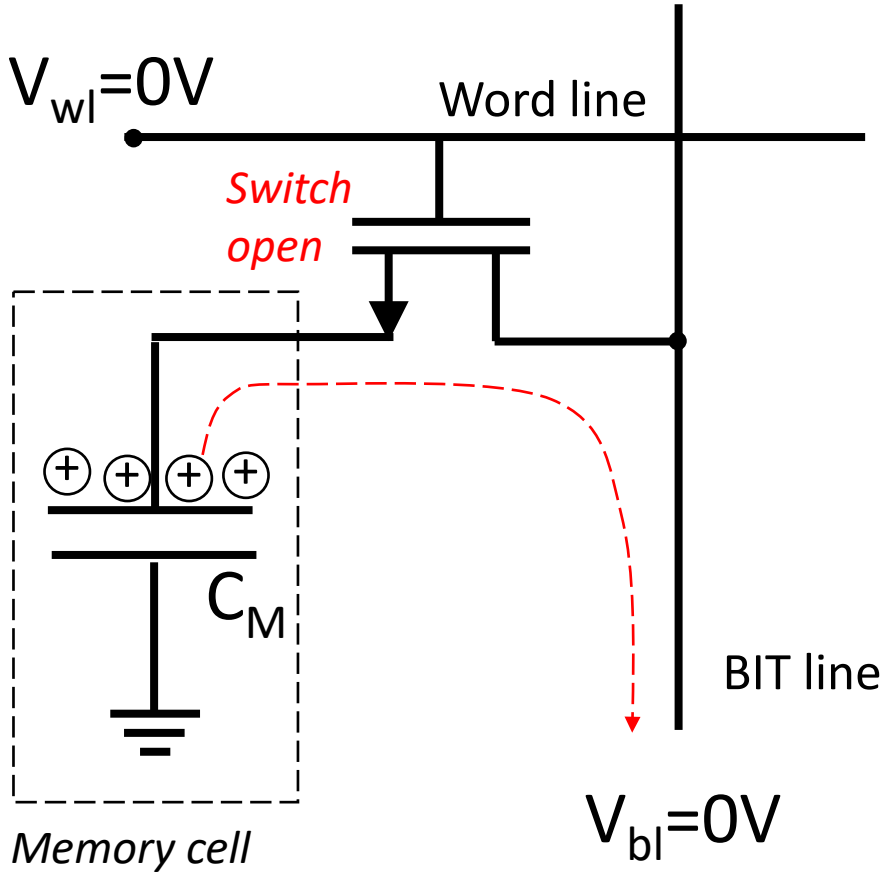


Random Access Memory (RAM) is popular because of its ability to access any location in memory with roughly the same time delay.

A DRAM cell is consists of only two components, a transistor, and a capacitor, both extremely small as billions can fit on a single memory chip, allowing for high densities at a lower cost.

When reading	Sense amplifier
When writing	delivering a charge to C_M

DRAM – Dynamic Random-Access Memory



When a MOSFET is OFF there are still very small currents

Charge in C_M «leaks» through the MOSFET to ground

Time to retain the information (τ) :

$$\tau = C_M \cdot R_{off} = 10fF \cdot 10^4 G\Omega = 0.1\ s\ !$$

C_M can not be made bigger because it will occupy too much area and cost too much.

This value is equivalent to about 100fA of leakage current

NEED of REFRESH
(every 100ms)

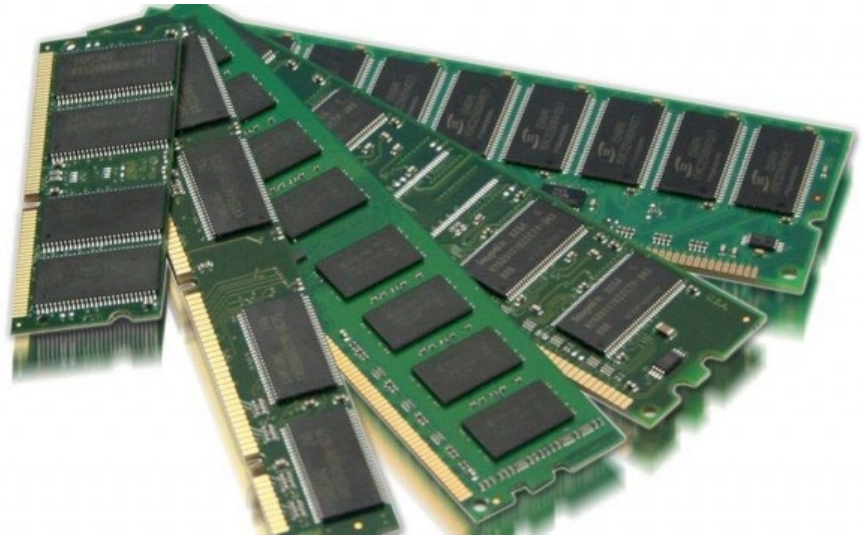
Because of the dynamic nature of memory cells, DRAM consumes a relatively large amount of power.

DRAM : summary

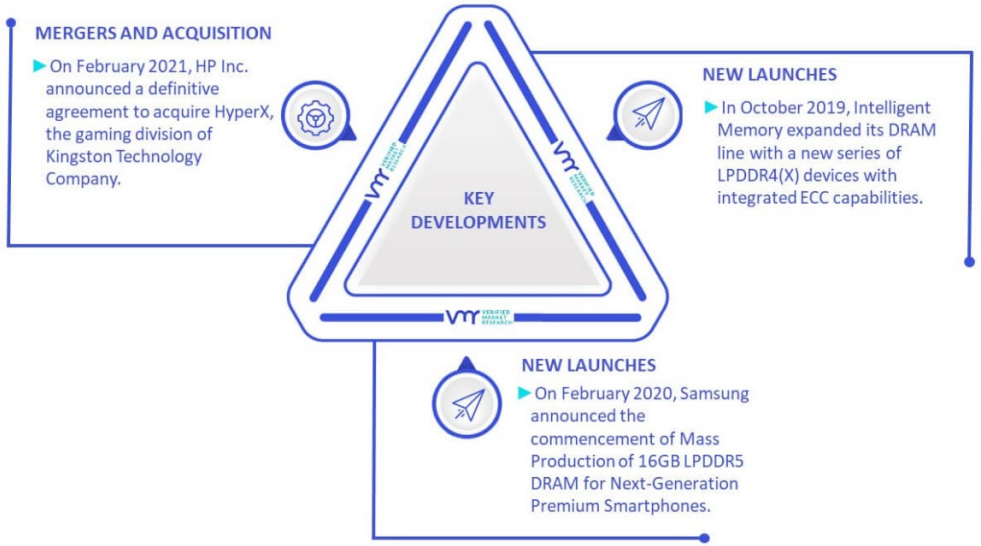
Is VOLATILE	Information disappears when Voltage supply is switched OFF
Is DYNAMIC	Need a refresh of the information (automatic and cycling reading of all the memory cells and refreshing)
Is RANDOM ACCESS	You can address every single memory cell (or a block of them) at your will in any moment
Is FAST	The data transfer rate for the 16GB LPDDR5 comes in at 5,500 megabits per second.

The LPDDR4 memories run at very high speeds with very low operating voltages and power consumption. They are made suitable for automotive applications, with design operability featuring higher temperature ranges up to 125°C and being AEC-Q100-qualified.

DRAM : market and players



The Dynamic Random Access Memory (DRAM) market was valued at USD 66.8 billion in 2020 and is expected to cross the USD 100 billion mark by the end of 2026 by witnessing a CAGR of approximately 7% for the period 2020-2026.



The major players are Samsung Electronics, SK HYNIX, Micron Technology, Kingston Technology, Nanya Technology, Winbond, Transcend Information.

End of the lesson